SEMICONDUCTOR MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-119512; filed June 12, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor memory device.

BACKGROUND

Generally, a NAND type flash memory in which memory cells are arranged in a three-dimensional shape is known.

An example of related art is JP-A-2006-12358.

DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a functional block of a memory system according to a first embodiment.

FIG. 2 illustrates a functional block of a memory according to the first embodiment.

FIG. 3 illustrates a block of the memory according to the first embodiment.

FIG. 4 illustrates a functional block of a sense amplifier module and a page buffer of the memory according to the first embodiment.

FIG. 5 illustrates elements and couplings of a part of the sense amplifier module and the page buffer of the memory according to the first embodiment.

FIG. 6 illustrates distributions of threshold voltages of cell transistors before and after write of two bits per cell transistor.

FIG. 7 illustrates a timing chart at the time of writing of the memory system according to the first embodiment.

FIG. 8 illustrates details of address signals which is used for the memory system according to the first embodiment.

FIG. 9 illustrates an example of a memory space that is recognized by a memory controller according to the first embodiment and an actual memory space of the memory.

FIG. 10 is an example of address signals necessary for designating a upper page and a lower page.

FIG. 11 illustrates a timing chart at the time of reading from the memory system according to the first embodiment.

FIG. 12 illustrates another timing chart at the time of reading from the memory system according to the first embodiment.

FIG. 13 illustrates a timing chart at the time of writing of a memory system for reference.

FIG. 14 illustrates another timing chart at the time of writing of the memory system for reference.

FIG. 15 illustrates elements and couplings of a part of a sense amplifier module and a page buffer of a memory according to a second embodiment.

FIG. 16 illustrates elements and couplings of another part of the sense amplifier module and the page buffer of the memory according to the second embodiment.

FIG. 17 illustrates a timing chart at the time of writing of a memory system according to the second embodiment.

FIG. 18 illustrates another timing chart at the time of writing of the memory system according to the second embodiment.

FIG. 19 illustrates a timing chart at the time of writing of a memory system for reference.

FIG. 20 illustrates another timing chart at the time of writing of the memory system for reference.

FIG. 21 illustrates elements and couplings of a part of a sense amplifier module and a page buffer of a memory according to a third embodiment.

FIG. 22 illustrates elements and couplings of a part of the memory according to the third embodiment.

FIG. 23 illustrates a timing chart at the time of writing of a memory system according to a third embodiment.

FIG. 24 illustrates a timing chart at the time of writing of a memory system for reference.

DETAILED DESCRIPTION

The present embodiment now will be described more fully hereinafter with reference to the accompanying drawings, in which various embodiments are shown. In the drawings, the thickness of layers and regions may be exaggerated for clarity. Like numbers refer to like elements throughout. As used herein the term “and/or” includes any and all combinations of one or more of the associated listed items and may be abbreviated as “ / ”.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms “a,” “an” and “the” are intended to include the plurality of forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises,” “comprising,” “having,” “includes,” “including” and/or variations thereof, when used in this specification, specify the presence of stated features, regions, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, steps, operations, elements, components, and/or groups thereof.

It will be understood that when an element such as a layer or region is referred to as being “on” or extending “onto” another element (and/or variations thereof), it may be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” or extending “directly onto” another element (and/or variations thereof), there are no intervening elements present. It will also be understood that when an element is referred to as being “connected” or “coupled” to another element (and/or variations thereof), it may be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element (and/or variations thereof), there are no intervening elements present.

It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, materials, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, material, region, layer or section from another element, material, region, layer or section. Thus, a first element, material, region, layer or section discussed below could be termed a second element, material, region, layer or section without departing from the teachings of the present invention.

Relative terms, such as “lower”, “back”, and “upper” may be used herein to describe one element's relationship to another element as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the structure in the Figure is turned over, elements described as being on the “backside” of substrate would then be oriented on “upper” surface of the substrate. The exemplary term “upper”, may therefore, encompasses both an orientation of “lower” and “upper,” depending on the particular orientation of the figure. Similarly, if the structure in one of the figures is turned over, elements described as “below” or “beneath” other elements would then be oriented “above” the other elements. The exemplary terms “below” or “beneath” can, therefore, encompass both an orientation of above and below.

Embodiments are described herein with reference to cross section and perspective illustrations that are schematic illustrations of idealized embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, a region illustrated or described as flat may, typically, have rough and/or nonlinear features. Moreover, sharp angles that are illustrated, typically, may be rounded. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region and are not intended to limit the scope of the present invention.

[0004]Embodiments provide a semiconductor memory device whose operation speed is increased.

[0005]In general, according to one embodiment, a semiconductor memory device includes a first data latch that is coupled to a memory cell and retains data with a plurality of bits; a second data latch that is coupled to the memory cell and retains data with a plurality of bits; a third data latch that is coupled to an input and output circuit and retains data with a plurality of bits; a fourth data latch that is coupled to the input and output circuit and retains data with a plurality of bits; a first data bus that couples the first data latch to the second data latch, and has a first width; and a second data bus that couples the third data latch to the first data bus, and has a width smaller than the first width.

[0007]Embodiments will be hereinafter described with reference to the drawings. In the following description, the same symbols or reference numerals will be attached to the configuration elements having substantially the same function and configuration, and repeated description thereof will be omitted. In addition, all of the description for a certain embodiment may be also applied to description for other embodiments, unless explicitly or apparently excluded.

First Embodiment

1-1. Configuration

[0008] FIG. 1 illustrates a functional block of a memory system according to a first embodiment. As illustrated in FIG. 1, the memory system 1 includes a NAND type flash memory (memory device, semiconductor memory device) 100, and a memory controller (controller) 200. The memory system 1 can further include a host apparatus 300.

[0009]The host apparatus 300 commands the controller 200 to perform an operation of reading from, writing to, erasing, or the like the memory 100.

[0010]The controller 200, controls the memory 100, based on a command from the host apparatus 300. The controller 200 includes a host interface circuit 201, a random access memory (RAM) 202, a central processing unit (CPU) 203, a buffer memory 204, and a NAND interface circuit 205. The host interface circuit 201 is coupled to the host apparatus 300 via a control bus, and is responsible for communication between the controller 200 and the host apparatus 300.

[0011]The NAND interface circuit 205 is coupled to the memory 100 via a NAND bus, and is responsible for communication between the controller 200 and the memory 100. The NAND bus includes an I/O bus. The I/O bus has a width of a plurality of bits (for example, eight bits), and transmits components, such as data, commands, and address signals. In addition, the NAND bus transmits various control signals. The control signals include a ready and busy signal. The ready and busy signal indicates whether the memory 100 is in a ready state or a busy state.

[0012]The CPU 203 controls the entire operations of the controller 200. The RAM 202 is used as a working area of the CPU 203. The buffer memory 204 temporarily retains data which is transmitted to the memory 100 and data which is transmitted from the memory 100.

[0013]The memory 100 includes a plurality of memory cells, and can store data in a non-volatile manner. For example, the memory 100 includes elements illustrated in FIG. 2. FIG. 2 illustrates a functional block of the memory according to a first embodiment. As illustrated in FIG. 2, the memory 100 includes a memory cell array 10, a sense amplifier module 11, a page buffer 12, a column decoder 13, a row decoder 14, an input and output circuit 15, a voltage generating circuit 16, and a sequencer 17.

[0014]The memory cell array 10 includes a plurality of (memory) blocks BLK (BLK0, BLK1, BLK2, …). Each of the blocks BLK includes a plurality of string units SU (SU0, SU1, SU2, …). Each of the string units SU includes a plurality of NAND strings NS. Each of the strings NS includes a plurality of memory cells. The memory cell array 10 includes wires, such as a bit line, and a word line.

[0015]The sense amplifier module 11 senses data, or temporarily retains the data.

[0016]The page buffer 12 retains read data and write data by a unit which is called a “page”. The size of one page is, for example, 16 KB, and this example will be used in the following description.

[0017]The column decoder 13 receives a column address signal, and controls coupling between a bit line and other elements, based on a column address. The row decoder 14 receives a row address signal, and applies various voltages to the word line, based on a row address.

[0018]The input and output circuit 15 is responsible for signal communication between the controller 200 and the memory 100.

[0019]The voltage generating circuit 16 includes, for example, a charge pump or the like, and generates voltages (potentials) required for writing, reading, and erasing of data. The voltage generating circuit 16 supplies the generated voltages to the sense amplifier module 11, the page buffer 12, the column decoder 13, the row decoder 14, and the like.

[0020]The sequencer 17 controls the entire operations of the memory 100.

[0021]the plurality of blocks BLK includes elements and couplings illustrated in, for example, FIG. 3. FIG. 3 illustrates a block of the memory according to the first embodiment. As illustrated in FIG. 3, each of the NAND strings NS includes a plurality of memory cell transistors MT (MT0 to MT7) which are coupled in series, and select gate transistors ST1 and ST2. The plurality of cell transistors MT retain data in a non-volatile manner. The plurality of cell transistors MT are coupled between ends of one side of the select gate transistors ST1 and ends of one side of the select gate transistor ST2.

[0022]Gates of the transistors ST1 included in the string unit SUx (x is zero, a natural number equal to or larger than “1”) are coupled to a select gate line SGDx. Gates of the transistors ST2 are coupled in common to a select gate line SGS.

[0023]In each of the string units SU, the other end of each transistors ST1 of the plurality of NAND strings NS is coupled to one of different bit lines BL (BL0 to BL(k-1)). The symbol K is a natural number, and for example, 16 KB. Each of the bit lines BL is coupled to each of the strings NS of different string units SU.

[0024]A control gates of a cell transistor MTm (m is zero or a natural number equal to or less than “7”) of the same block BLK is coupled to the word line WLm. Writing and reading of data is collectively performed to and from a set (set of cells) of the cell transistors MT which are coupled to one word line WL of one string unit SU. The memory space of the set of the cells includes one or more pages. One page may be configured by a memory space of a part of the transistors MT among the set of cells. The memory 100 can retain data equal to or more than two bits in one cell transistor MT. If the data with two bits per cell transistor MT is retained, a set of upper bits of each of the cell transistors MT sharing the word line WL of one string unit SU is referred to as a upper page, and a set of lower bits is referred to as a lower page.

[0025]The memory cell array 10 may have a different configuration. The configuration of the memory cell array 10 is disclosed in, for example, U.S. patent application No. 12/407,403 filed March 19, 2009, entitled “three-dimensionally stacked non-volatile semiconductor memory”. In addition, the memory cell array 10 is disclosed in U.S. patent application No. 12/406,524 filed March 18, 2009, entitled “three-dimensionally stacked non-volatile semiconductor memory”. Furthermore, the memory cell array 10 is disclosed in U.S. patent application No. 12/679,991 filed March 25, 2010, entitled “non-volatile semiconductor memory device and method of manufacturing the same”, and U.S. patent application No. 12/532,030 filed March 23, 2009, entitled “semiconductor memory and method of manufacturing the same”. The entire contents of the above patent applications are employed in the present specification by reference.

[0026]The sense amplifier module 11 and the page buffer 12 have elements and couplings illustrated in, for example, FIG. 4. FIG. 4 illustrates a functional block of the sense amplifier module and the page buffer according to the first embodiment. As illustrated in FIG. 4, the sense amplifier module 11 includes a sense amplifier SA. The sense amplifier SA is coupled to the bit line BL, senses the data which is read on the bit line BL, and transmits write data to the bit line BL. The sense amplifier SA can perform sensing and transmitting of data by a size of one page. The sense amplifier SA includes a plurality of sense amplifier groups SAU. Each sense amplifier group SAU senses and transmits data with a plurality of bits (for example, 16 bits. This example will be used in the following description).

[0027]The sense amplifier module 11 further includes data latches SDL, LDL, and UDL. The data latches SDL, LDL, and UDL can respectively retain data with a size of one page. The data latch SDL includes a plurality of data latch groups SDLU. Each data latch group SDLU can retain data with a plurality of bits (for example, 16 bits). In the same manner, the data latch UDL includes a plurality of data latch groups UDLU. Each data latch group UDLU can retain data with a plurality of bits (for example, 16 bits). Furthermore, the data latch LDL also includes a plurality of data latch groups LDLU. Each data latch group LDLU can retain data with a plurality of bits (for example, 16 bits).

[0028]The page buffer 12 includes two data latches XDL0 and XDL1. The data latches XDL0 and XDL1 can respectively retain data with a size of one page. For example, the data latch XDL0 includes a plurality of data latch groups XDL0U. Each data latch group XDL0U can retain data with a plurality of bits (for example, 16 bits). The data latch XDL1 includes a plurality of data latch groups XDL1U. Each data latch group XDL1U can retain data with a plurality of bits (for example, 16 bits).

[0029]One sense amplifier group SAU, one data latch group SDLU, one data latch group LDLU, and one data latch group UDLU are coupled to each other by a data bus LBUS. The data bus LBUS has a width of 16 bits. For this reason, the data latch group SDLU, the data latch group LDLU, and the data latch group UDLU can transmit and receive in parallel the data with 16 bits to and from each other.

[0030] The one sense amplifier group SAU, the one data latch group SDLU, the one data latch group LDLU, and the one data latch group UDLU are coupled to the one data latch group XDL0 and the one data latch group XDL1 by a data bus DBUS. The data bus DBUS has a width of 1 bit. For this reason, the data latch groups SDLU, LDLU, and UDLU transmit and receive the data with one bit at a time to and from the data latch group XDL0. In the same manner, the data latch groups SDLU, LDLU, and UDLU transmit and receive the data with one bit at a time to and from the data latch group XDL1.

[0031]The sense amplifier group SAU, and the data latch groups SDLU, LDLU, UDLU, XDL0U, and XDL1U which are coupled by the data buses LBUS and DBUS configure one set. By the set of sense amplifier group SAU, and the data latch groups SDLU, LDLU, UDLU, XDL0U, and XDL1U, the data with 16 bits is handled.

[0032]The sense amplifier group SAU, and the data latch groups SDLU, LDLU, UDLU, XDL0U, and XDL1U have elements and couplings which are illustrated in FIG. 5. FIG. 5 illustrates elements and couplings of one set of the sense amplifier group SAU, and the data latch groups SDLU, LDLU, UDLU, XDL0U, and XDL1U.

[0033]The set of the sense amplifier group SAU, and the data latch groups SDLU, LDLU, and UDLU include 16 units U (U[0] to U[15]).

[0034]Each unit U is coupled to one bit line BL, and includes one sense amplifier circuit SAC, one data latch circuit SDLC, one data latch circuit LDLC, and one data latch circuit UDLC. The one sense amplifier circuit SAC senses data which is read on the coupled bit line BL, and transmits write data to the coupled bit line BL. The one data latch circuits SDLC, LDLC, and UDLC respectively retain data with one bit. In the unit U[n] (n is zero or a natural number equal to or less than “15”), the one sense amplifier circuit SAC and the one data latch circuits SDLC, LDLC, and UDLC can be coupled respectively and selectively to the data bus LBUS[n] by transmission gates, and can be coupled to each other via the data bus LBUS[n]. The data buses LBUS[0] to LBUS[15] can be all coupled selectively to the data bus DBUS.

[0035]Each data latch group XDL0U includes data latch circuits XDLOC[0] to XDLOC[15]. Each of the data latch circuits XDL0C[0] to XDL0C[15] can be selectively coupled to the data bus DBUS.

[0036] Each data latch group XDL1U includes data latch circuits XDL1C[0] to XDL1C[15]. Each of the data latch circuits XDL1C[0] to XDL1C[15] can be selectively coupled to the data bus DBUS.

[0037]Elements accompanied by common [n] in the end relate to each other, and data is transmitted between the related elements. That is, for example, the data latch circuit XDLOC[0] transmits and receives data to and from the data latch circuits SDLC[0], UDLC[0], and LDLC[0], and the data latch circuit XDL1C[1] transmits and receives data to and from the data latch circuits SDLC[1], UDLC[1], and LDLC[1].

[0038]Furthermore, the data bus DBUS is coupled to the data bus IOBUS. Coupling between the data bus IOBUS and the data bus DBUS is controlled by the column decoder 13. The data bus IOBUS is coupled to the input and output circuit 15 of FIG. 2. Write data from the outside of the memory 100 is first received by the data latch XDL0 or XDL1. In the same manner, it is necessary for read data from the cell transistor MT to be transmitted to the data latch XDL0 or XDL1, so as to be output to the outside of the memory 100.

1-2. Operation

[0039]An example of the operation of the memory system 1 according to the first embodiment will be described hereinafter. Operations of the controller 200 and the memory 100 at the time of writing and reading, among various operations of the memory system 1, will be described. The following description is made based on retention of data with two bits per cell transistor MT. Hence, a method of retaining the data with two bits per cell transistor MT will be first described with reference to FIG. 6. FIG. 6 illustrates distributions of threshold voltages of cell transistors before and after write of two bits per cell transistor.

[0040]The threshold voltage of each cell transistor MT is set to any one of four values according to the data to be retained. A plurality of cell transistors MT which retain the data with the same two bits can also have threshold voltages different from each other. For this reason, the threshold voltages have distributions. The threshold voltages are referred to as, for example, an E level, an A level, a B level, and a C level. (a) of FIG. 6 illustrates a state (erasing state) before data is written. As illustrated in (a) of FIG. 6, the cell transistor MT is in an “E” level.

[0041](b) of FIG. 6 illustrates a state in which data is written. As illustrated in (b) of FIG. 6, the cell transistor MT is in the E level, the A level, the B level, or the C level. The threshold voltage in the A level is higher than that in the E level. The threshold voltage in the B level is higher than that in the A level. The threshold voltage in the C level is higher than that in the B level.

[0042]The four levels relate to four states of data with two bits. An example of the relation is as follows. The cell transistor MT in E level is handled as in a state in which data of “1” is retained in upper bits and lower bits. The cell transistor MT in A level is handled as in a state in which data of “1” is retained in the upper bits and data of “0” is retained in the lower bits. The cell transistor MT in B level is handled as in a state in which data of “0” is retained in upper bits and lower bits. The cell transistor MT in C level is handled as in a state in which data of “0” is retained in the upper bits and data of “1” is retained in the lower bits.

[0043]Writing to a state of (b) of FIG. 6 in which only the lower page (lower bit) does not pass through the written state from a state of (a) of FIG. 6, is referred to as full sequence write.

[0044]Read includes calculation of threshold voltages of each cell transistors MT. For example, the calculation of the threshold voltages includes calculation indicating whether or not each cell transistor MT of a target of the calculation is in any one of the E level, the A level, the B level, and the C level. The calculation of the level of the cell transistor MT includes comparison of the threshold voltage of the cell transistor MT and read voltages VA, VB, and VC. The voltage VB is higher than the voltage VA, and the voltage VC is higher than the voltage VB.

[0045]The cell transistor MT having the threshold voltage lower than the voltage VA is calculated to be in the E level. The cell transistor MT having the threshold voltage which is equal to or higher than the voltage VA and is lower than the voltage VB is calculated to be in the A level. The cell transistor MT having the threshold voltage which is equal to or higher than the voltage VB and is lower than the voltage VC is calculated to be in the B level. The cell transistor MT having the threshold voltage equal to or higher than the voltage VC is calculated to be in the C level.

1-2-1. Writing

[0046]Referring to FIG. 7, an example of operations of the controller 200 and the memory 100 at the time of writing will be described. FIG. 7 illustrates a timing chart at the time of writing according to the first embodiment, and relates to an example of writing of a full sequence.

[0047]As illustrated in FIG. 7, the controller 200 transmits a write command 80h and an address signal Add via the I/O bus at time t1. The address signal designates two page addresses, to which data is written, in the memory space of the memory 100. The two pages that are a write destination are a upper page and a lower page which are formed by a set of the (entire) cell transistors MT coupled to one word line WL in one string unit SU. Due to the designation of the two pages, the address signal first designates one block BLK, one string (string unit SU), and one word line WL. Furthermore, the address signal specifies that the write data which is transmitted after the write command has a size of two pages. An example for this method will be described hereinafter with reference to FIG. 8.

[0048]FIG. 8 illustrates details of the address signal which is used in the memory system according to the first embodiment. FIG. 8 is based on an example in which the controller 200 and the memory 100 include I/O bus with an eight-bit width and transmit the address signal according to five input cycles. In the figure, I/O0 to I/O7 configure the I/O bus, and each of I/O0 to I/O7 transmits data with one bit. Thus, FIG. 8 is based on an example in which the address signal with 40 bits of A0 to A39 is transmitted.

[0049]As illustrated in FIG. 8, for example, a column address is transmitted according to each of I/O0 to I/O7 (A0 to A15) of first and second input cycles. The column address designates a column of an access target. One column corresponds to 16 bits which are handled by a set of the sense amplifier group SAU, and the data latch groups SDLU, LDLU, UDLU, XDL0U, and XDL1U illustrated in FIG. 4.

[0050]For example, it is possible to specify one column from among columns (=2 KB) of double columns (=16 KB/16=1 KB) in one page, according to the column address. This leads the controller 200 to recognize that one page has a double size (=16 KB´2) of a size of actual one page of the memory 100. Thus, if each cell transistor MT stores two bits, the controller 200 recognizes that a set of cell transistors MT coupled to one word line WL retains one page which is configured by a set of the upper page and the lower page formed by the transistors MT. Specifically, as illustrated in FIG. 9, the actual memory space of the memory 100 includes a page with a size of 16 KB of 2p pieces, and in contrast to this, the memory space of the memory 100 which is recognized by the controller 200 includes a page with a size of 32 KB of p pieces. If one write data has a size of one page differently from the present embodiment, the column address signal designates a column of a size of one page.

[0051]The description returns to FIG. 8. A string address is transmitted according to I/O0 and I/O1 (A16 to A16) of a third input cycle. The string address designates the string (string unit SU) of an access target. In addition, a word line address is transmitted according to I/O2 to I/O7 (A18 to A23) of the third cycle. The word line designates the word line WL of an access target.

[0052]A plane address is transmitted according to I/O0 (A24) of a fourth input cycle. The plane address designates a plane of an access target, if the memory 100 includes a plurality of planes. The plane includes a set of the memory cell array 10, the sense amplifier module 11, the page buffer 12, the column decoder 13, and the row decoder 14.

[0053]A block address is transmitted according to I/O1 to I/O7 of the fourth input cycle and I/O0 to I/O3 of a fifth input cycle which are A25 to A35. The block address designates the block BLK of an access target. A chip address is transmitted according to I/O4 to I/O6 (A36 to A38) of the fifth input cycle. The chip address designates the memory 100 of an access target, if the memory system includes a plurality of the memories 100.

[0054]The column address can designate columns of bit numbers equal to the size of two pages, and thus the address signal does not require assignment of bits for designating the upper page or the lower page. In this case, as illustrated in FIG. 10, it is possible to exclude that information for designating the upper or lower page is assigned to a certain bit (for example A16), and to shift a subsequent bit (after A17) to a bit before one bit. FIG. 10 illustrates an example of an address signal which requires designation of the upper page and the lower page.

[0055]The description returns to FIG. 7. The controller 200 transmits data (LowerDIN) to be written to the lower page at time t2 to the memory 100. Furthermore, the controller 200 transmits data (UpperDIN) to be written to the upper page to the memory 100, after the data LowerDIN. The data LowerDIN is retained in one (for example, data latch XDL0. The following description uses this example) of the two data latches XDL0 and XDL1, by the sequencer 17. The data UpperDIN is retained in the other (for example, data latch XDL1. The following description uses this example) of the two data latches XDL0 and XDL1. At a time point in which write starts, the data latches XDL0 and XDL1 do not retain any valid data, and can receive write data.

[0056]The data LowerDIN and UpperDIN are continuously transmitted, and a boundary between the data LowerDIN and the data UpperDIN is not specified. For this reason, the sequencer 17 starts first to retain the received data to the data latch XDL0 as soon as the data is received. If retaining of the data with a size of one page in the data latch XDL0 is completed, the sequencer 17 starts to retain different data with a size of one page which is subsequent to the received data with a size of one page, in the data latch XDL1, at the same time as a start of reception. Thus, a portion (data LowerDIN) with a size of one page is retained in the data latch XDL0 from the head of the data with a size of two pages, and a subsequent portion (data UpperDIN) with a size of one page is retained in the data latch XDL1. The sequencer 17 recognizes which one of the data latches XDL0 and XDL1 retains the data LowerDIN or UpperDIN.

[0057]The controller 200 further transmits a command 10h to the memory 100 after the data UpperDIN. The command 10h instructs a start of full sequence write. The sequencer 17 recognizes the instruction of the start of the full sequence write, based on that the command 10h is received by the memory 100. Specifically, the sequencer 17 recognizes that the data with a size of two pages is written by the full sequence write to a memory space of the set of the cell transistors MT coupled to the designated word line WL of the designated string unit SU of the block BL designated by the address signal Add. If receiving the command 10h, the memory 100 enters a busy state at time t3, and indicates the busy state according to the ready and busy signal R/B.

[0058]The full sequence write includes operations, such as pump setup (PMP ON), data transfer, write, pump recovery, and the like. The pump setup indicates generation of a voltage required for writing performed by the voltage generating circuit 16, and includes generation of a voltage which is applied to the word line WL and the select gate lines SGD and SGS, and generation of a voltage required for an operation of the data bus DBUS. The pump recovery (PMP RCV) indicates initialization of the voltage generating circuit 16.

[0059]The data transfer includes transfer of the data LowerDIN in the data latch XDL0 to one (for example, data latch LDL. The following description uses this example) of the data latches SDL, UDL, and LDL (X to L), and transfer of the data UpperDIN in the data latch XDL1 to another (for example, data latch UDL. The following description uses this example) of the data latches SDL, UDL, and LDL (X to U).

[0060]The write includes applying a predetermined potential to the word line WL and the select gate lines SGD and SGS, verifying the written data, and the like. As the result of write, the data is written to the upper page and the lower page which is designated by the address of write destination. That is, the sequencer 17 calculation whether each of the cell transistors coupled to the word line (selected word line) selected (designated) by the data LowerDIN and UpperDIN has to be maintained to the E level, or has to be written to any one of the A level, the B level, and the C level. Subsequently, the sequencer 17 maintains each cell transistor MT coupled to the selected word line WL to the E level by using a control of the sense amplifier module 11 and the row decoder 14, or sets each cell transistor MT to a threshold voltage of the A, B, or C level. If the write and verification of data is completed, the sequencer 17 performs the pump recovery. If the pump recovery is completed, the sequencer 17 indicates the ready state according to the ready and busy signal R/B. Thus, the write operation which is performed by the controller 200 and the memory 100 is completed.

1-2-2. Reading

[0061]Referring to FIG. 11 and FIG. 12, an example of the operations of the controller 200 and the memory 100 at the time of reading will be described. FIG. 11 and FIG. 12 illustrate timing charts at the time of reading the memory system according to the first embodiment.

[0062]The reading includes two methods. In first reading, both the upper page and the lower page in a memory space of a set of the cell transistor MT coupled to one word line WL are designated by one set of commands. In second reading, only the upper page or only the lower page in a memory space of a set of the cell transistor MT coupled to one word line WL is designated by one set of commands. FIG. 11 is based on an example of the first reading, and FIG. 12 is based on an example of the second reading.

[0063]In the first reading, as illustrated in FIG. 11, the controller 200 transmits a reading command 00h and the address signal Add to the memory 100 at time t11. The command 00h indicates reading the cell transistor MT coupled to the word line WL designated by a subsequent address signal Add. In the same manner as the writing, the address signal Add designates at least one of the columns of a size of two pages using the column address (refer to FIG. 8). Subsequently, the controller 200 transmits a command 30h to the memory 100. The command 30h indicates a start of reading.

[0064]If the memory 100 receives the command 30h, the sequencer 17 performs the pump setup at time t12, and subsequently, performs reading. The reading includes applying a predetermined potential to the word line WL and the select gate lines SGD and SGS, or the like. The reading includes calculation of the threshold voltage of each cell transistor MT (of reading target) coupled to the designated word line WL.

[0065]FIG. 11 illustrates an example of calculation of the sequence of the A level, the B level, and the C level. First of all, the sequencer 17 calculates whether or not the cell transistor MT of a reading target has a threshold voltage equal to or higher than the voltage VA (A reading (AR)). The cell transistor MT having a threshold voltage lower than the voltage VA is calculated as in the E level. Subsequently, the sequencer 17 calculates whether or not the cell transistor (cell transistor of B reading target) MT excluding the cell transistor which is calculated as in the E level among the cell transistors of all the reading targets has a threshold voltage equal to or higher than the voltage VB (B reading (BR)). The cell transistor MT having a threshold voltage lower than the voltage VB among the cell transistors MT of the B reading target is calculated as in the A level.

[0066]In the same manner, the sequencer 17 calculates whether or not the cell transistor (cell transistor of C reading target) MT excluding the cell transistor MT which is calculated as in the E or A level among the cell transistors MT of all the reading targets has a threshold voltage equal to or higher than the voltage VC (C reading (BR)). The cell transistor MT having a threshold voltage lower than the voltage VC among the cell transistors MT of the C reading target is calculated as in the B level, and the cell transistor MT having a threshold voltage equal to or higher than the voltage VC is calculated as in the C level.

[0067]The sequencer 17 produces read data LowerDOUT of the lower page and read data UpperDOUT of the upper page, using the level of the calculated cell transistor MT. The data LowerDOUT includes a set of values of lower bits of each cell transistor MT among the set of the cell transistors MT of reading target. The data UpperDOUT includes a set of values of higher bits of each cell transistor MT among the set of the cell transistors MT of reading target. The data LowerDOUT is retained in, for example, the data latch LDL. The data UpperDOUT is retained in, for example, the data latch UDL.[0068]Subsequently, the sequencer 17 transmits the data LowerDOUT in the data latch LDL to one (for example, XDL0. The following description uses this example) of the two data latches XDL0 and XDL1, at time t13. Furthermore, the sequencer 17 transmits the data UpperDOUT in the data latch UDL to the other (for example, XDL1. The following description uses this example) of the two data latches XDL0 and XDL1. The data LowerDOUT and UpperDOUT in the data latches XDL0 and XDL1 is transmitted to the controller 200 according to the control of the sequencer 17. Subsequently, the sequencer 17 performs the pump recovery, and completes the reading.

[0069]In the second reading, as illustrated in FIG. 12, the controller 200 transmits a prefix command XXh or YYh before the reading command 00h to the memory 100. The prefix command XXh indicates that the reading command 00h instructs reading from the lower page subsequently. The prefix command YYh indicates that the reading command 00h instructs reading from the upper page subsequently.

[0070] If receiving the command XXh or 00h, the memory 100 reads data from the lower page of the set of the cell transistors MT designated by the subsequent address signal Add1. Details of the data read from the lower page become different depending on assignment of values to a certain level, higher bits, and lower bits. An example based on the example of FIG. 6 is as follows. The sequencer 17 performs the A reading and the C reading. As a result of the A and C reading, the cell transistor MT in the E level or the C level is specified. The cell transistor MT in the E level or the C level retains one piece of data in the lower bits. Based on this, the data LowerDOUT of the lower page is generated. The generated data LowerDOUT is retained in, for example, the data latch LDL, then is transmitted to the data latch XDL0, and is transmitted to the controller 200.

[0071]Meanwhile, if the commands YYH and 00h are continuously received, the memory 100 reads data from the upper page of the set of the cell transistors MT designated by the subsequent address signal Add2. Details of the data read from the upper page become different depending on assignment of values to a certain level, higher bits, and lower bits. An example based on the example of FIG. 6 is as follows. The sequencer 17 performs the B reading. As a result of the B reading, the cell transistor MT in the E level or the A level is specified. The cell transistor MT in the E level or the A level retains one piece of data in the higher bits. Based on this, the data UpperDOUT of the upper page is generated. The generated data UpperDOUT is retained in, for example, the data latch UDL, then is transmitted to the data latch XDL1, and is transmitted to the controller 200.

[0072]The reading the upper page or the lower page corresponds to the reading the first half or the second half of the page of a size of 16 KB´2 of the set of the cell transistors MT coupled to the word line WL designated by the controller 200.

1-3. Effect (Advantage)

[0073]According to the first embodiment, the following effects are obtained. First of all, for comparison, an example of the full sequence write to the memory having only one data latch (for example, data latch XDL) for input and output of the data to and from the memory will be described with reference to FIG. 13. As illustrated in FIG. 13, the controller transmits a write command UUh, the address signal Add1, the data LowerDIN, and a command WWh to the memory. The address signal Add1 designates a block, a string, a word line, and the upper page or the lower page. The received data LowerDIN is retained in the data latch XDL. The command WWh indicates that data of one page is transmitted. If the command WWh is received, the memory performs the pump setup, transmits the data LowerDIN to the data latch (for example, data latch LDL) (X to L), and performs the pump recovery. After transmission of the data LowerDIN is completed, the data latch XDL can receive data again.

[0074]If the memory is in a ready state, the controller transmits a write command UUh, the address signal Add2, the data UpperDIN, and a command ZZh to the memory. The received data LowerDIN is retained in the data latch XDL. The command ZZh indicates a start of the full sequence write. The memory receives the command ZZh, performs the pump setup, and transmits the data UpperDIN to the data latch (for example, data latch UDL) (X to U). As a result, a start of the full sequence write is ready, and then memory performs the full sequence write.

[0075]Meanwhile, according to the first embodiment, the memory 100 includes the two data latches XDL0 and XDL1 coupled to the data bus IOBUS. For this reason, the memory 100 does not require transmission to a data latch (data latch LDL or UDL, or the like) different from the data latches XDL0 or XDL1, and can retain the data of two pages in the data latches XDL0 and XDL1. Thus, the memory 100 can continuously (following one write command) receive the data of two pages for the full sequence write. This excludes the need for transmission of the write command UUh twice, as illustrated in a comparison example of FIG. 13. As a result, as can become apparent from the comparison with FIG. 13, the first embodiment only requires the pump setup of one time and the pump recovery of one time. As a result, the time required for the full sequence write according to the first embodiment is reduced compared to that of the example of FIG. 13.

[0076]The same effects can also be obtained from the reading. That is, in the continuous reading of two pages of the controller and the memory of the example for comparison, two read commands 00h are not required to be transmitted, as illustrated in FIG. 14. For this reason, the pump setup and the pump recovery are required for each of the lower page reading and the upper page reading.

[0077]Meanwhile, according to the first embodiment, the pump setup of one time and the pump recovery of one time are required for reading of two pages, as can be seen from FIG. 11. For this reason, the time required for the continuous reading of two pages according to the first embodiment is reduced compared to that of the example of FIG. 14.

[0078]Furthermore, according to the first embodiment, it is possible to read the lower page or the upper page, according to the introduction of the prefix commands XXh and YYh. In the reading of three of more continuous pages, instructing the reading of the upper page and the lower page by one write command is more efficient than the reading of FIG. 14. Meanwhile, in the reading of only the upper or lower page, the reading of FIG. 12 is more efficient than the reading of FIG. 11. It is all possible to perform the two readings, and thus convenience of the memory 100 is increased.

Second Embodiment

[0079]A NAND type flash memory according to a second embodiment will be described with reference to FIG. 15 to FIG. 20.

2-1. Configuration

[0080]The NAND flash memory according to the second embodiment is different from that of the first embodiment in configurations of the sense amplifier module 11 and the page buffer 12. The other configurations are the same as those of the first embodiment.

[0081]The sense amplifier module 11 and the page buffer 12 according to the second embodiment include elements and couplings illustrated in FIG. 15. FIG. 15 illustrates a functional block of the sense amplifier module 11 and the page buffer 12 according to the second embodiment. As illustrated in FIG. 15, in the second embodiment, one sense amplifier group SAU, one data latch group SDLU, one data latch group LDLU, and one data latch group UDLU are coupled to one data latch group XDL0U by a data bus DBUS0, and are coupled to one data latch group XDL1U by a data bus DBUS1. The data buses DBUS0 and DBUS1 have widths of one bit.

[0082]FIG. 16 illustrates details of one sense amplifier group SAU, one data latch group SDLU, one data latch group LDLU, one data latch group UDLU, one data latch group XDL0U, and one data latch group XDL1U.

[0083]Data buses LBUS[0] to LBUS[15] can all be selectively coupled to the data bus DBUS0, and can all be selectively coupled to the data bus DBUS1.

[0084]The data bus DBUS0 is coupled to a data bus DBUS0a via a switch SW11. The data bus DBUS0a has a width of one bit, and in addition, can be selectively coupled to each of data latch circuits XDL0C[0] to XDL0C[15]. The data bus DBUS0a is further coupled to the data bus IOBUS via the switch SW12.

[0085]The data bus DBUS1 is coupled to a data bus DBUS1a via a switch SW21. The data bus DBUS1a has a width of one bit, and in addition, can be selectively coupled to each of data latch circuits XDL1C[0] to XDL1C[15]. The data bus DBUS1a is further coupled to the data bus IOBUS via the switch SW22.

[0086]The switches SW11, SW12, SW21, and SW22 are, for example, metal oxide semiconductor field effect transistors (MOSFET), and are turned on or off by the column decoder 13 and the sequencer 17. The switch SW11 is turned on to couple the data latch XDL0 (that is, the data bus DBUS0a) to the data bus DBUS0 (furthermore, data bus LBUS[0] to LBUS[15])). The switch SW12 is turned on to couple the data bus DBUS0a to the data bus IOBUS. The switch SW21 is turned on to couple the data latch XDL1 (that is, the data bus DBUS1a) to the data bus DBUS1 (furthermore, data bus LBUS[0] to LBUS[15])). The switch SW22 is turned on to couple the data bus DBUS1a to the data bus IOBUS. While one of the switches 11 and Sw21 is turned on, the other is maintained to be off. While one of the switches 12 and Sw22 is turned on, the other is maintained to be off.

2-2. Operation

[0087]An example of an operation of a memory system 1 according to a second embodiment will be described as follows. Particularly, operations of the controller 200 and the memory 100 at the time of two writings will be described. First writing is a normal writing. Second writing is writing in which interrupt processing is included during writing.

2-2-1. Example of First Writing

[0088]An example of the first writing will be described with reference to FIG. 17. FIG. 17 illustrates a timing chart at the time of writing of the memory system according to the second embodiment. One writing command 80h instructs writing of data with a size of one page, and is based on an example of instruction of continuous writing of a plurality of pages. At the time of a start of writing, both the data latches XDL0 and XDL1 do not retain data.

[0089]As illustrated in FIG. 17, the controller 200 transmits the write command 80h and the address signal Add1 to the memory 100 via the I/O bus, at time t31. The address signal Add1 designates a write destination of write data Data1 following the address signal Add1, and specifically, designates one word line WL of one string of one block, and the lower page or the upper page. If the data Data1 is receive by the memory 100, the data Data1 is retained in a vacant data latch of the data latches XDL0 and XDL1 under a control of the sequencer 17. For example, the data Data1 is retained in the data latch XDL0. If output of the data Data1 is completed, the controller 200 transmits a command 15h to the memory 100. Furthermore, the command 15h indicates presence of the write data.

[0090]If the memory 100 receives the command 15h, the sequencer 17 starts writing of the data Data1 at time t32. As a part of this operation, the sequencer 17 performs various calculations using the data Data1 of the data latch XDL0. For performing the calculation, the sequencer 17 transmits the data Data1 of the data latch XDL0 to any one of the data latches SDL, UDL, and LDL. The transmission may be performed several times. The data Data1 in the data latch XDL0 is continuously retained up to time t35. In addition, the data Data1 is continuously written up to time t37, and the data Data1 is written to the designated cell transistor MT.

[0091]If the memory 100 receives the command 15h, the memory 100 is in a busy state at time t32, but immediately returns to a ready state at time t33. The data latch XDL0 still retains the data, data transmission from the data latch XDL0 and writing of the data Data1 also continue at time t33, and the memory 100 can further receive the write data from the data latch XDL1.

[0092]The controller 200 recognizes that the memory 100 is in a ready state, and transmits the next write command 80h to the memory 100, after time t33. Subsequently, the controller 200 transmits the address signal Add2, the write data Data2, and the command 15h to the memory 100. If the memory 100 receives the data Data2, the data Data2 is retained in a vacant one (the data latch XDL1 in the present example) of the data latches XDL0 and XDL1 under a control of the sequencer 17. If output of the write data Data2 is completed, the controller 200 transmits the command 15h to the memory 100 at time t34. Based on this, the sequencer 17 writes the data Data2 to the designated cell transistor MT at time t37, in the same manner as the data Data1. Also during the writing, the data Data2 is continuously retained in the data latch XDL1.

[0093]If the command 15h is received, the memory 100 enters the busy state. The busy state continues until retention of the data Data1 in the data latch XDL0 is completed (time t35). The reason is that the data is retained in the data latches XDL0 and XDL1, and the memory 100 cannot further receive data. If the data latch XDL0 is released at time t35, the memory 100 enters the ready state.

[0094] The controller 200 recognizes that the memory 100 is in a ready state, and performs transmission of a command for write data Data3, an address signal Add3, and the data, at time t36. The data Data3 is retained in the data latch XDL0 which completes retention of data at time t35. An operation of the data Data3 at time t36 and thereafter is the same as that of the data Data1 or Data2.

2-2-2. Example of Second Writing

[0095] An example of second writing will be described with reference to FIG. 18. FIG. 18 illustrates a timing chart at the time of writing of a memory system according to the second embodiment. As illustrated in FIG. 18, the controller 200 transmits the write command 80h, the address signal Add1, and the write data Data1 to the memory 100 at time t41. If the memory 100 starts to receive the data Data1, the sequencer 17 starts to retain the write data Data1 in a vacant one (for example, the data latch XDL0. The following description uses this example) of the data latches XDL0 and XDL1.

[0096]Subsequently, the controller 200 receives instruction of data reading from, for example, the host apparatus 300, before writing according to the write command 80h is completed. Based on the instruction, the controller 200 stops transmission of the data Data1 at time t42. At a point of time t42, the data latch XDL0 retains part Data1(a) of a head of the write data Data1 which is already received, and continuously retains the part.

[0097]In addition, the controller 200 transmits a read command X0h to the memory 100 at time t42. The read command X0h can be generated before the preceding write command 80h, and the subsequent address signal and a write start command (for example, command 15h) are transmitted. That is, the memory 100 recognizes the read command X0h which is received after the write command 80h is received and before a pair of write start commands 15h is received, as a command which is generated in accordance with a correct sequence.

[0098]The controller 200 transmits the address signal Add2 and a read start command 30h to the memory 100 following a command X0h. The address signal Add2 designates an address of a read source.

[0099]If the memory 100 receives the command 30h, the sequencer 17 reads the data Data2 from the designated address. The data Data2 is read to any one of the data latches SDL, UDL, and LDL, and furthermore, is transmitted to a vacant one (data latch XDL1, in the present example) of the data latches XDL0 and XDL1 in preparation for output from the memory 100.

[0100]The controller 200 recognizes that time is required for preparing output of the read data from the memory 100 after the command 30h is transmitted. Hence, the controller 200 performs a restart of transmission of the write data Data1, using the time for the preparation. Specifically, the controller 200 transmits data Data1(b) to the memory 100 via the I/O bus at time t43 after the command 30h is transmitted. The data1(b) is a part following the data Data1(a) of the data Data1. The sequencer 17 recognizes that that data Data1(b) is data of a write target according to the write command 80h and is a part subsequent to the data Data1(a), based on the fact that the write start command 15h pairing with the write command 80h is not yet received. Based on this, the sequencer 17 retains the data Data1(b) in a part following the data Data1(a) of the data latch XDL0.

[0101]At time t44 after transmission of the data Data1(b), the controller 200 transmits the command X1h to the memory 100. The command X1h indicates that transmission of a part data (data Data1(b)) of the data Data1 is completed and transmission of other parts of the data Data1 is not completed. The sequencer 17 recognizes that the data Data2 can be output according to completion of the transmission of the data Data1(b) to the memory 100, based on reception of the command X1h. Based on this, the sequencer 17 transmits the data Data2 of the data latch XDL1 to the controller 200 via the I/O bus, from time t45.

[0102]If receiving of the read data Data2 is completed, the controller 200 restarts the transmission of the write data Data1. For this reason, the controller 200 transmits a command X2h to the memory 100 at time t46. The command X2h indicates a start of the transmission of a subsequent data Data1(c), and indicates that the data Data1(c) is a part following the part (data Data1(b)) which is finally transmitted, among the data Data1. The controller 200 transmits the data Data1(c) to the memory 100 according to the command X2h. If the memory 100 receives the data Data1(c), the data Data1(c) is retained in a part following the data Data1(b) of the data latch XDL0 under the control of the sequencer 17. Thus, the write data Data1 is all retained in the data latch XDL0.

[0103]If the transmission of the data Data1 is completed, the controller 200 transmits the write start command 15h to the memory 100. If the memory 100 receives the command 15h, the sequencer 17 writes the write data Data1 of the data latch XDL0 to the cell transistor MT designated by the address signal Add1.

[0104]FIG. 18 illustrates an example in which the data latch XDL1 also retains the data Data2 after the data Data2 is output. Based on the example, the memory 100 enters the busy state after receiving the command 15h. The reason is that the data latches XDL0 and XDL1 retain the data. Thus, after the data Data2 is output, the data latch XDL1 may be released. By doing so, the memory 100 rapidly returns to the ready state after receiving the command 15h, and can perform additional operation using the data latch XDL1.

2-2-3. Others

[0105]In the configuration of the second embodiment, the operation of the first embodiment can also be performed. That is, at the time of writing, data of a upper page and a lower page for full sequence writing is continuously received by the memory 100 after one write command. At the time reading, one of the data of the upper page and the data of the lower page is retained in one of the data latches XDL0 and XDL1, and the other is retained in the other of the data latches XDL0 and XDL1, in response to one read command.

2-3 Effect (Advantage)

[0106] According to the second embodiment, the following effects are obtained. First of all, for comparison, an example of continuous writing to a plurality of pages with respect to a memory having only one data latch (for example, data latch XDL) for input and output will be described with reference to FIG. 19. As illustrated in FIG. 19, if receiving the data Data1 and the command 15h, the memory 100 enters a busy state at time t52. For calculation using the data Data1, a repeated transmission of the data Data1 to the data latches SDL and LDL or UDL is required, and for this reason, the data latch XDL is used by the data Data1. In addition, writing of the data Data1 to the cell transistor starts at time t52.

[0107]The controller is required to postpone transmission of the next write command and data, until the data latch XDL is released and thereby the memory enters the ready state. If need for retaining the data Data1 in the data latch XDL disappears and the memory enter the ready state at time t53, the controller transmits the write command 80h, the address signal Add2, and the data Data2 to the memory. If receiving the write data Data2, the memory transmits the data Data2 for writing to the data latches SDL and LDL or UDL and starts writing. However, if a size of the data Data2 is large, time for receiving the data Data2 in the data latch XDL may be increased, and a start of transmission to the data latches SDL and LDL, or UDL and a start of writing may be delayed. The transmission and the writing start from time t55.

[0108]Meanwhile, writing of the data Data1 is ended from time t54 prior to time t55. For this reason, although the memory can start writing from time t54, the memory has standby time from time t54 to time t55, since preparation for writing of the data Data2 is not completed. The standby time is due to the fact that transmission of the write data Data2 from the controller to the memory is postponed.

[0109]Meanwhile, according to the second embodiment, the memory 100 includes the two data latches XDL0 and XDL1 which are coupled to the data bus IOBUS. For this reason, also while one data latch XDL0 is used by a certain data, the memory can receive other data from the controller 200 using the other data latch XDL1. Thus, as can be seen from FIG. 17, after the write start command 15h is received, the memory 100 immediately enters the ready state from time t33, and can receive the next write command 80h and the data Data2. For this reason, at a time point in which writing of the data Data1 is completed from time t37, preparation for writing of the data Data2 is completed. Thus, writing of the data Data2 can be started following the completion of writing of the data Data1. As a result, time required for continuous writing to a plurality of pages performed by the memory 100 is reduced compared to that of FIG. 19.

[0110]In addition, interrupt of reading during transmission of the write data to the memory is also the same. First of all, for comparison, an example of interrupt of reading during transmission of the write data with respect to the memory having only one data latch (for example, data latch XDL) for input and output to and from the memory will be described with reference to FIG. 20. As illustrated in FIG. 20, from time t62, if receiving a read command Y0h before all of the write data Data1 is received, the memory performs an operation for releasing the data latch XDL in preparation for the read data. That is, the sequencer transmits a received part of the data Data1 of the data latch XDL to the data latches SDL and LDL, or UDL, from time t63. Since the data latches SDL and LDL, or UDL is used for the transmission, the data cannot be read from the cell transistor of a read source, and standby time from time t63 to time t64 is generated.

[0111]If transmission of the data Data1 is completed, the sequencer starts reading of the data Data2 from the cell transistor of a read source at the following time t64. The data Data2 which is read is transmitted from the data latch XDL to the controller. Subsequently, the sequencer transmits a part of the write data Data1 of the data latches SDL and UDL, or LDL to the data latch XDL, based on the fact that the memory receives the command Y2h. If the transmission is completed, the controller transmits the rest part of the data Data1 from time t66, after a command Y3h indicating a restart of transmission of the write data Data1 is transmitted.

[0112]In this way, transmission of the data Data1 from the data latch XDL and transmission of the data to the data latch XDL are required, and during the transmission, standby time is generated. Since the data latch XDL and the data latches SDL and LDL, or UDL are coupled by the data bus with a width of one bit, data transmission between the data latch XDL and the data latches SDL and LDL, or UDL requires a long time. Thus, operation speed of the memory is decreased due to a plurality of transmissions which require a long time.

[0113]Meanwhile, according to the second embodiment, as can be seen from FIG. 18, it is not necessary for the memory 100 to transmit the data Data1(a) of the data latch XDL0 to the data latches SDL and LDL, or UDL, for data reading. For this reason, the memory 100 can start to read the data Data2 from the cell transistors MT, immediately after the read command X0h of interrupt is received. Thus, if reading is instructed during transmission of the write data to the memory, the time required until reading is completed is reduced compared to that of FIG. 20.

Third Embodiment

[0114]A NAND type flash memory according to a third embodiment will be described with reference to FIG. 21 to FIG. 24. The third embodiment is based on the second embodiment, and the memory 100 further includes an XOR (exclusive logical sum) logic circuit between sense amplifier module 11 and the page buffer 12.

3-1. Configuration

[0115]The NAND type flash memory according to the third embodiment is different from that of the second embodiment in configurations of the sense amplifier module 11 and the page buffer 12. The other configurations are the same as those of the second embodiment.

[0116]The memory 100 includes couplings of the sense amplifier module 11 and the page buffer 12 illustrated in FIG. 21, and includes elements and couplings illustrated in FIG. 21 between the sense amplifier module 11 and the page buffer 12. FIG. 21 illustrates the sense amplifier module 11, the page buffer 12, and only the portions related to 16 bit lines BL among portions between the sense amplifier module 11 and the page buffer 12. In the same manner as in the first and second embodiments, a configuration illustrated in FIG. 21 is provided with respect to each of a plurality of sets of the 16 bite lines BL.

[0117]As illustrated in FIG. 21, the memory 100 further includes an XOR logic circuit 50 and a random number seed generating unit 50g. The XOR logic circuit 50 randomizes write data. In addition, the XOR logic circuit 50 recovers the data (that is, write data received from the controller 200 at the time of writing) before randomization from the data received from the cell transistors MT.

[0118]An end of a data bus DBUS0a which is opposite to the switch SW12 is coupled to the XOR logic circuit 50 instead of the switch SW11 of the second embodiment (FIG. 17). An end of a data bus DBUS1a which is opposite to the switch SW22 is coupled to the XOR logic circuit 50 instead of the switch SW21 of the second embodiment. In addition, the XOR logic circuit 50 is coupled to a data bus DBUS2 via the switch SW11. The data bus DBUS2 has a width of one bit and can be selectively coupled to data buses LBUS[0] to LBUS[15] by a transmission gate. The XOR logic circuit 50 receives a random number seed from the random number seed generating unit 50g.

[0119]The XOR logic circuit 50 has the configuration illustrated in, for example, FIG. 22. FIG. 22 illustrates elements and couplings of a part of a memory according to the third embodiment. As illustrated in FIG. 22, the XOR logic circuit 50 includes a randomization circuit 51 and a decoding circuit 52.

[0120]The randomization circuit 51 includes N type MOSFETs NMOS0 and NMOS1, and switches SW01, SWo2, and SW03. The switches SW01, SW02, and SW03 are, for example, MOSFETs. Ends of each of the transistors NMOS0 and NMOS1 are coupled to a node A via the switch SW03. The node A is coupled to the bus DBUS2 via the switch SW11. The other end of the transistor NMOS0 is coupled to a data bus DBUS0a via the switch SW01, and is coupled to a gate of the transistor NMOS1. The other end of the transistor NMOS1 is coupled to a data bus DBUS1a via the switch SW02, and is coupled to a gate of the transistor NMOS0.

[0121]The decoding circuit 52 includes MOSFETs NMOS3 and NMOS4, and switches SW10, SW20, and SW30. The switches SW10, SW20, and SW30 are, for example, MOSFETs. One end of the transistor NMOS4 is coupled to the node A via the switch SW30. The other end of the transistor NMOS4 is coupled to a data bus DBUS1a via the switch SW10. A gate of the transistor NMOS4 is coupled to the data bus DBUS0 via the switch SW20. The transistor NMOS3 is coupled between the other end of the transistor NMOS4 and the gate of the transistor NMOS4. A gate of the transistor NMOS3 is coupled to the data bus DBUS2 via the switch SW30.

[0122]The switches SW01, SW02, SW03, SW10, SW20, SW30, SW40, and SW41 are controlled by the sequencer 17.

[0123]The data bus DBUS0a is coupled to the node A via the switch SW40, so as to be able to bypass the randomization circuit 51 and the decoding circuit 52. In the same manner, the data bus DBUS1a is coupled to the node A via the switch SW41, so as to be able to bypass the randomization circuit 51 and the decoding circuit 52.

[0124]The random number seed generating unit 50g is coupled to the node A.

3-2. Operation

[0125]First of all, an operation of the XOR logic circuit 50 will be described prior to description of an operation of the memory system 1.

[0126]There is a case in which randomization of a sequence of bits is performed for the write data, which is received by the memory 100, from the controller 200, in order to relax uneven distributions of bits of “1” and bits of “0” of a bit string of the data. By relaxing the uneven distributions, reliability of the write data is increased. The randomization is performed by using the randomization circuit 51.

[0127]The randomized write data is retained in the data latch XDL1. In order to randomize, the sequencer 17 turns on the switch SW03, turns off the switch SW30, and retains random number seeds from the random number seed generating unit 50g in the data latch XDL0 by controlling the random number seed generating unit 50g. For example, the random number seed includes a bit string of the number equal to the number of bits of one page. The random number seeds are arranged in the order in which bits of “1” and “0” in the bit string are randomly determined. Thus, a value (“0” or “1” of data) of one bit is retained to disposition which is randomly determined, in each of the data latch circuits XDL0C[0] to XDL0C[15].

[0128]Hereinafter, the configuration illustrated in FIG. 22 will be described. However, an operation of the following description is also performed in parallel in the portions which have the same configurations as in FIG. 22 and are different from FIG. 22.

[0129]During randomization, the switches SW10, SW20, SW30, SW40, and SW41 are maintained to be off, the switch SW11 is maintained to be on. In addition, at a time point of the start of the randomization, the switch SW01, SW02, and SW03 are turned off.

[0130]The sequencer 17 repeatedly performs an operation with respect to one bit of the write data with respect to each of 16 bits, and performs the operation with respect to 16 bits which are processed by the configuration of FIG. 21, which will be described below. A sequence of the processing of 16 bits is arbitrary. The sequencer 17 performs randomization, using, for example, the data latch circuits LDLC[0] to LDLC[15]. During the randomization, the data latch circuits UDLC[0] to UDLC[15] and LDLC[0] to LDLC[15] are electrically decoupled from the data buses LBUS[0] to LBUS[15].

[0131]First of all, the sequencer 17 electrically decouples the data latch circuit LDLC[n] from the data bus LBUS[n]. Subsequently, the sequencer 17 precharges a potential of the data bus DBUS2 to a high level. The high level of the potential of the data bus DBUS2 relates to “1” data.

[0132]The sequencer 17 couples the data latch circuit XDL0C[0] to the data bus DBUS0a, and couples the data latch circuit XDL1C[0] to the data bus DBUS1a. As a result, a potential of the data bus DBUS0a is maintained to have a low level in accordance with the data of the data latch circuit XDL1C[0], but goes up to a high level. In addition, a potential of the data bus DBUS1a is maintained to have a low level in accordance with the data of the data latch circuit XDL0C[0], but goes up to a high level. Both the data latch circuits XDLC[0] and XDLC[1] retain, for example, “0” data, and thus both the data buses DBUS0a and DBUS1a are maintained to have a low level.

[0133]In this state, the sequencer 17 turns on the switches SW01, SW02, and SW03, thereby enabling the randomization circuit 51. As a result, the data bus DBUS2 is maintained to have a high level or goes down to a low level, according to the state of the data buses DBUD0a and DBUS1a. In the present example, the transistor NMOS0 and NMOS1 are maintained to be off, and thus the data bus DBUS2 is maintained to have a high level.

[0134]Subsequently, the sequencer 17 couples the data latch circuit LDLC[0] to the data bus DBUS2. As a result, “1” data is retained in the data latch circuit LDLC[0]. Accordingly, the data retained in the data latch circuit LDLC[0] is inverted data of an exclusive logical sum of the data of the data latch circuit XDL1C and the data of the data latch circuit XDL0C.

[0135]If the two the data latch circuits XDL0C[n] and XDL1C[n] retain “1” data, the transistors NMOS1 and NMOS2 are turned on. As a result, the data bus DBUS2 is coupled to the data buses DBUS0a and DBUS1a, but is maintained to have a high level. Thus, “1” data is retained in the corresponding data latch circuit LDLC[n].

[0136]Meanwhile, if the data latch circuit XDL0C[n] retains “0” data and the data latch circuit XDL1C[n] retains “1” data, the transistor NMOS0 is turned on and the transistor NMOS1 is turned off. As a result, the data bus DBUS2 is coupled o the data bus DBUS0a, and goes down to a low level. Thus, “1” data is retained in the corresponding data latch circuit LDLC[n]. Even if the data latch circuit XDL0C[n] retains “1” data and the data latch circuit XDL1C[n] retains “0” data, “1” data is retained in the corresponding data latch circuit LDLC[n].

[0137]Retaining the exclusive logical sum of the data of the data latch circuit XDL0C[y] (y is “0” or a natural number equal to or less than 15) and the data of the data latch circuit XDL1C[y] in the data latch circuit LDLC[y] is performed with respect to each of “0” to “15” of y. Accordingly, the data retained in the data latch circuits LDLC[0] to LDLC[15] is data in which a sequence of bits of a part of the write data retained in the data latch circuits XDLC[0] to XDLC[15] is randomized.

[0138]Meanwhile, the data which is read from the cell transistors MT is decoded (randomization is released) by using the decoding circuit 52. In the following description, the configuration illustrated in FIG. 22 will be described in the same manner as the description with regard to the randomization, but the operation described below is performed also in the portions which have the same configurations as in FIG. 22 and are different from FIG. 22.

[0139]During decoding, the switches SW10, SW20, SW30, and SW11 are maintained to be on, and the switches SW01, SW02, SW03, SW40, and SW41 are maintained to be off.

[0140]First of all, the data with an amount of one page which is read from the cell transistors MT is retained in the data latch LDL. Subsequently, the sequencer 17 turns off the switch SW03, turns on the switch SW30, and retains random number seeds from the random number seed generating unit 50g in the data latch XDL0 by controlling the random number seed generating unit 50g. The random number seed is the same as that to be used at the time of randomizing, and each bit of the random number seed is retained in each of the data latch circuits XDL0C[0] to XDL0C[15]. At a time point of the start of the decoding, any data latch circuit XDL1C of the data latches XDL1 also retains “1” data.

[0141]In the same manner as the randomization, the sequencer 17 repeatedly performs the operation of one bit of the write data with respect to each of 16 bits, and performs the operation with respect to 16 bits which are processed by the configuration of FIG. 21, which will be described below.

[0142]If the data latch circuit LDLC[y] retains “1” data and the data latch circuit XDL0C[y] retains “1” data, “1” data is continuously retained in the data latch circuit XDLC[y]. If the data latch circuit LDLC[y] retains “1” data and the data latch circuit XDL0C[y] retains “0” data, “0” data is retained in the data latch circuit XDL1C[y]. If the data latch circuit LDLC[y] retains “0” data and the data latch circuit XDL0C[y] retains “1” data, “0” data is retained in the data latch circuit XDL1C[y]. If the data latch circuit LDLC[y] retains “0” data and the data latch circuit XDL0C[y] retains “0” data, “1” data is continuously retained in the data latch circuit XDL1C[y].

[0143] Retaining the exclusive logical sum of the data of the data latch circuit XDL1C[y] and the data of the data latch circuit XDL0C[y] in the data latch circuit LDLC[y] is performed with respect to each of “0” to “15” of y. As a result, the data which is read from the cell transistors MT of a read source and whose randomization is released is retained in the data latch XDL0.

[0144]Next, an example of the operation of the memory system 1 will be described with reference to FIG. 23. FIG. 23 illustrates a timing chart at the time of writing of the memory system 1 according to the third embodiment.

[0145]As illustrated in FIG. 23, the controller 200 transmits the write command 80h, the address signal Add1, and the write data Data1 to the memory 100 from time t71. The address signal Add1 designates a write destination. If the memory 100 receives the data Data1, the data Data1 is retained in the data latch XDL1, and is continuously retained thereafter.

[0146]If the memory 100 receives a write start command 10, the sequencer 17 generates the random number seed by controlling the random number seed generating unit 50g, from time t72. The random number seed is transmitted to the data latch XDL0, is retained in the data latch XDL0, and is continuously retained thereafter.

[0147]If transmission of the random number seed to the data latch XDL0 is completed, the sequencer 17 randomizes the data Data1 by using the random number seed from time t73, and transmits the randomized data Data1 to the data latch LDL. Subsequently, the sequencer 17 writes the data of the data latch LDL to the designated cell transistors MT.

3-3. Effect (Advantage)

According to the third embodiment, the memory 100 includes the two data latches XDL0 and XDL1 which are coupled to the data bus IOBUS, in the same manner as in the second embodiment. For this reason, the same advantages as those of the second embodiment are obtained.

[0148]Furthermore, according to the third embodiment, the following advantages are obtained. First of all, for comparison, an example of writing accompanied by randomization in the memory having only one data latch (for example data latch XDL) for input and output will be described with reference to FIG. 24.

[0149]As illustrated in FIG. 24, if the data latch XDL completes reception of the write data Data1, the sequencer transmits the data Data1 to the data latch UDL thereby releasing the data latch XDL. If the data latch XDL is released, the sequencer transmits the random number seed to the data latch XDL. Subsequently, the sequencer performs calculation of a logical product of an inverted bit of each bit of the bit string of the random number seed and a corresponding bit of the data Data1, with respect to the entire bits of one page, and transmits the calculation result to the data latch LDL. In addition, the sequencer performs calculation of a logical product of each bit of the random number seed and a corresponding bit of the data Data1, with respect to the entire bits of the data with a size of an amount of one page, and transmits the calculation result to the data latch SDL. Finally, the sequencer performs calculation of a logical sum of the data of the data latch LDL and the data of the data latch SDL, with respect to each bit, and transmits the calculation result to the data latch UDL. The data of the data latch UDL which is obtained by doing so is an exclusive logical sum of the write data Data1 and the random number seed.

[0150]As can be seen from FIG. 24, three transmissions from the data latch XDL to the data latches UDL, LDL, and SDL are required. As described above, the data bus DBUS had a width of one bit, and thus data transmission between the data latch XDL and the data latches SDL and LDL, or UDL requires a long time.

[0151]Meanwhile, according to the third embodiment, since the memory 100 includes two data latches XDL0 and XDL1 coupled to the data bus IOBUS, the data transmission from the data latch XDL occurs only once from time t73 and thereafter, as can be seen from FIG. 23. For this reason, according to the third embodiment, the time required for the writing accompanying the data randomization is reduced compared to that in FIG. 24.

Other Embodiments

[0152]In the first to third embodiments, the following operation and configuration may be used.

[0153](1) In read operations of multi-value levels, a voltage which is applied to a word line selected at a read operation of an A level is between, for example, 0 V and 0.55 V. The embodiments are not limited to this, and the voltage may be any one between 0.1 V and 0.24 V, 0.21 V and 0.31 V, 0.31 V and 0.4 V, 0.4 V and 0.5 V, 0.5 V and 0.55 V, and the like. A voltage which is applied to a word line selected at a read operation of a B level is between, for example, 1.5 V and 2.3 V. The embodiments are not limited to this, and the voltage may be any one between 1.65 V and 1.8 V, 1.8 V and 1.95 V, 1.95 V and 2.1 V, 2.1 V and 2.3 V, and the like. A voltage which is applied to a word line selected at a read operation of a C level is, for example, 3.0 V to 4.0 V. The embodiments are not limited to this, and the voltage may be any one between 3.0 V and 3.2 V, 3.2 V and 3.4 V, 3.4 V and 3.5 V, 3.5 V and 3.6 V, 3.6 V and 4.0 V, and the like. The time (tR) of the read operation may be any one between, for example, 25 ms and 38 ms, 38 ms and 70 ms, 70 ms and 80 ms, and the like.

[0154]The write operation includes a program operation and a verification operation. In the write operation, a voltage which is initially applied to a word line selected at the time of program operation is between, for example, 13.7 V and 14.3 V. The embodiments are not limited to this, and the voltage may be any one between, for example, 13.7 V and 14.0 V, 14.0 V and 14.6 V, and the like. A voltage which is initially applied to a word line selected at the time of writing to odd-numbered word lines may be different from a voltage which is initially applied to a word line selected at the time of writing to even-numbered word lines. When the program operation uses an incremental step pulse program (ISPP) method, for example, a voltage of approximately 0.5 V may be used as a step-up voltage. For example, a voltage of 6.0 V to 7.3 V may be used as a voltage which is applied to a non-selected word line. The embodiments are not limited to this, and the voltage may be any one between, for example, 7.3 V and 8.4 V, and may be 6.0 V or less may be used. Pass voltages to be applied may vary depending on whether the non-selected word line is an odd-numbered word line or an even-numbered word line. Any one between, for example, 1700 ms and 1800 ms, 1800 ms and 1900 ms, and 1900 ms and 2000 ms may be used as the time (tProg) of the write operation.

[0155](3) In an erase operation, a voltage that is initially applied to a well which is disposed on an upper portion of a semiconductor substrate and in which memory cells are disposed on an upper side is between, for example, 12V and 13.6 V. The embodiments are not limited to this, and the voltage may be any one between, for example, 13.6 V and 14.8 V, 14.8 V and 19.0 V, 19.0 V and 19.8 V, 19.8 V and 21 V, and the like. Any one between, for example, 3000 ms and 4000 ms, 4000 ms and 5000 ms, and 5000 ms and 9000 ms may be used as the time (tErase) of the erase operation.

[0156](4) the memory cell may have the following configuration. The memory cell includes a charge accumulation film which is disposed on a semiconductor substrate of a silicon substrate or the like via a tunnel insulating film with a thickness of 4 nm to 10 nm. The charge accumulation film may have a stacked structure of an insulating film, such as a silicon nitride (SiN) film with a thickness of 2 nm to 3 nm or a silicon oxynitride (SiON) film, and a polysilicon (Poly-Si) film with a thickness of 3 nm to 8 nm. A metal such as ruthenium (Ru) may be contained in the polysilicon film. The memory cell has an insulating film on the charge accumulation film. The insulating film includes a silicon oxide (SiO) film with thickness of 4 nm to 10 nm which is interposed between, for example, a lower layer High-k film with a thickness of 3 nm to 10 nm and an upper layer High-k film with a thickness of 3 nm to 10 nm. A hafnium oxide (HfO) or the like may be used as a material of the High-k film. In addition, a thickness of the silicon oxide film may be greater than that of the High-k film. A control electrode with a thickness of 30 nm to 70 nm is provided on the insulating film via a film for work function adjustment with thickness of 3 nm to 10 nm. The film for work function adjustment is, for example, a metal oxide film such as tantalum oxide (TaO), a metal nitride film such as tantalum nitride (TaN), or the like. The control electrode may use tungsten (W) or the like. An air gap may be formed between the memory cells.

[0157]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a first data latch that is coupled to a memory cell and retains data with a plurality of bits;

a second data latch that is coupled to the memory cell and retains data with a plurality of bits;

a third data latch that is coupled to an input and output circuit and retains data with a plurality of bits;

a fourth data latch that is coupled to the input and output circuit and retains data with a plurality of bits;

a first data bus that couples the first data latch to the second data latch, and has a first width; and

a second data bus that couples the third data latch to the first data bus, and has a width smaller than the first width.

2. The device according to Claim 1,

wherein the first to fourth data latches are respectively configured by i columns, and

wherein the semiconductor memory device recognizes a signal that designates at least one of 2´i columns.

3. The device according to Claim 1, wherein the second data bus further couples the fourth data latch to the first data bus.

4. The device according to Claim 1, further comprising:

a third data bus that couples the fourth data latch to the first data bus, and has a with smaller than the first width.

5. The device according to Claim 4, further comprising:

a logic circuit that is provided between the first data bus and the third and fourth data latches.

ABSTRACT

According to one embodiment, a semiconductor memory device includes a first data latch that is coupled to a memory cell and retains data with a plurality of bits; a second data latch that is coupled to the memory cell and retains data with a plurality of bits; a third data latch that is coupled to an input and output circuit and retains data with a plurality of bits; a fourth data latch that is coupled to the input and output circuit and retains data with a plurality of bits; a first data bus that couples the first data latch to the second data latch, and has a first width; and a second data bus that couples the third data latch to the first data bus, and has a width smaller than the first width.

Drawings

FIG. 2

118: NAND string

15: ROW DECODER

11: SENSE AMPLIFIER MODULE

12: PAGE BUFFER

13: COLUMN DECODER

14: INPUT AND OUTPUT CIRCUIT

16: VOLTAGE GENERATING CIRCUIT

17: SEQUENCER

FIG. 4

ONE COLUMN (16 bits)

TO CELL ARRAY

ONE PAGE

TO INPUT AND OUTPUT CIRCUIT

FIG. 5

13: COLUMN DECODER

FIG. 7

INSIDE OF MEMORY

WRITING

TIME

FIG. 9

MEMORY SPACE (PAGE) OF MEMORY THAT IS RECOGNIZED BY CONTROLLER

p PIECES

PAGE

ACTUAL MEMORY SPACE (PAGE) OF MEMORY

2p PIECES

PAGE

FIG. 11

INSIDE OF MEMORY

TIME

FIG. 12

INSIDE OF MEMORY

TIME

FIG. 13

INSIDE OF MEMORY

WRITING

TIME

FIG. 14

INSIDE OF MEMORY

TIME

FIG. 15

ONE COLUMN (16 bits)

TO CELL ARRAY

ONE PAGE

TO INPUT AND OUTPUT CIRCUIT

FIG. 16

13: COLUMN DECODER

FIG. 17

INSIDE OF MEMORY

Data1 WRITING

Data2 WRITING

TIME

FIG. 18

INSIDE OF MEMORY

Data2 READING

Data1 WRITING

TIMEFIG. 19

INSIDE OF MEMORY

Data1 WRITING

Data2 WRITING

TIME

FIG. 20

INSIDE OF MEMORY

Data1 (ADDITION)

Data2 READING

Data1 WRITING

TIME

FIG. 21

50: XOR LOGIC CIRCUIT

13: COLUMN DECODER

FIG. 22

50: XOR LOGIC CIRCUIT

FIG. 23

INSIDE OF MEMORY

SEED GENERATION

Data1 TRANSMISSION

Seed TRANSMISSION

WRITING

TIME

FIG. 24

INSIDE OF MEMORY

SEED GENERATION

Data1 TRANSMISSION

Seed TRANSMISSION

WRITING

TIME